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APPLICATION OF FIELD-EFFECT TRANSISTORS TO R-F POWER GENERATION

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APPLICATION OF FIELD-EFFECT TRANSISTORS TO R-F POWER GENERATION

by

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[redacted]

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ABSTRACT

Field effect transistors have several characteristics which are distinct from those of standard bipolar transistors. In this paper a study is made to see if any of these characteristics can be advantageously utilized to generate r-f power.

A conventional class-C FET r-f power amplifier is analyzed following a semigraphical method similar to that used for vacuum tubes. Some advantageous characteristics of the device are discussed along with some drawbacks.

The applicability of FETs to pulse-excited r-f power generation circuits is investigated and the device limitations in this field of application are discussed.

Finally, the combined use of an FET and a conventional bipolar transistor, to overcome the respective limitations, in an efficient r-f power generation circuit is studied. A practical working model of this hybrid circuit was built to illustrate its advantages.

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SYMBOLS AND ABBREVIATIONS

BV_{GDO}	Gate to Drain Breakdown Voltage with Source Open
BV_{GDS}	Gate to Drain Breakdown Voltage with Source Connected to Drain
BV_{GSS}	Gate to Source Breakdown Voltage with Drain Shorted to Source
E_d	Amplitude of Varying Component of v_d
E_g	Amplitude of Varying Component of v_g
e_g	Varying Component of v_g
E_{d1}	Amplitude of Fundamental Component of v_d
i_c	Varying Component of Collector Current
i_d	Varying Component of Drain Current
i_b	Varying Component of Base Current
I_D	dc Drain Current
I_{DSS}	Drain Current with Gate Shorted to Source
I_{GSS}	Gate-to-Source Current with Drain Shorted to Source
i_{ds}	Total Drain Current
I_p	Peak Drain or Collector Current During the Cycle
I_{g1}	Amplitude of the Gate Current Fundamental Component
I_{gdc}	dc Gate Current
I_{GSB}	Gate-to-Source Current with Substrate Shorted to Source
g_{fs}	Common Source Forward Transconductance
R_s	Saturation Resistance
V_{DD}	FET Drain Supply Voltage
V_{CC}	Bipolar Transistor Collector Supply
v_d	Total Drain Voltage
v_g	Total Gate Voltage
V_{DS}	dc Drain-to-Source Voltage

SYMBOLS AND ABBREVIATIONS

V_p	Pinch-Off Voltage
V_s	Saturation Voltage
v_{gmax}	$E_g - \lvert V_{GG} \rvert$
V_{GG}	Gate-to-Source Bias Supply
V_{EE}	Exciter Power Supply
V_L	Peak Load Voltage

1. Introduction

Field effect transistors (FETs) possess several superior characteristics over the bipolar transistors which are useful in some applications. Some of the characteristics of FETs distinct from those of the standard transistors are their high input impedances; low noise figures; low sensitivity to radiation and ambient temperature changes. [11] These are not the only characteristics inherent to FETs. Many more intrinsic operating characteristics suggest ingenious electronic circuits for particular applications. One such example is an FET micropower amplifier operating at extremely low power levels with very high voltage gain; 60 decibels of voltage gain at a power drain of less than 100 microwatts. [14] This amplifier circuit is developed from a less apparent characteristic of certain FETs, i.e., a higher ratio of transconductance to drain current at low values of drain current.

Although FETs have an extensive history and many application notes are found in the literature, there seems to be no discussions on the use of this device as an r-f power generator. With this and the above mentioned as a motivating factor, the FET in r-f power generation circuits is studied in some detail with particular attention paid to the advantageous use of device characteristics.

As for the vacuum tube and the bipolar transistor counterparts, the efficiency of the device and the circuitry becomes a significant factor in the r-f power generation problem, particularly if the output power level is relatively high. There are many applications in which amplitude linearity between input and output is not necessary. This fact makes class-C or equivalent operation of r-f power amplifiers possible and at the same time enhances the overall system efficiency.

The overall efficiency of the system is improved through the fulfillment of the customary design objectives of a class-C or equivalent r-f power amplifiers; i.e., (1) high device efficiency, (2) large available power output with a given device, and (3) low excitation power required for proper operation.

The study results given in the subsequent sections show that the FET used as an r-f power generator is inferior to the conventional bipolar transistors as far as power output and collector efficiency are concerned. These are the prime factors of the overall amplifier efficiency. This conclusion is drawn from the investigations of several devices and from technical articles available to the writer during the course of study. This claim is based on the present state-of-the art of FET design and production.

Although the drain efficiency of the device is poor, the device has some advantages which are discussed in the pertinent sections. Moreover, the advantage of the FET becomes pronounced when it is used with a conventional high efficiency switching power transistor in a suitable circuit configuration. With this hybrid circuit concept, all of the design objectives of the class-C or equivalent r-f power amplifiers mentioned above can be achieved. This is illustrated by the test results of an appropriate circuit.

2. Basic Operation and Characteristics of FETs

A unipolar field effect transistor is a semiconductor current path device whose conductivity is modulated by an applied transverse electric field. The main distinction between the operating mechanism of the conventional bipolar transistor and the FET is that the current flow through the device is predominantly by only one type of carrier in the case of an FET, while both majority and minority carriers are involved in the case of the conventional transistor. Hence the term, "unipolar", refers to the FETs; and "bipolar" to the conventional transistors. Expressed differently, bipolar transistors are current controlled devices while the unipolar FETs are voltage controlled devices. This difference of controlling the current through the device is shown in Fig. 1 for the common emitter and the common source configuration.

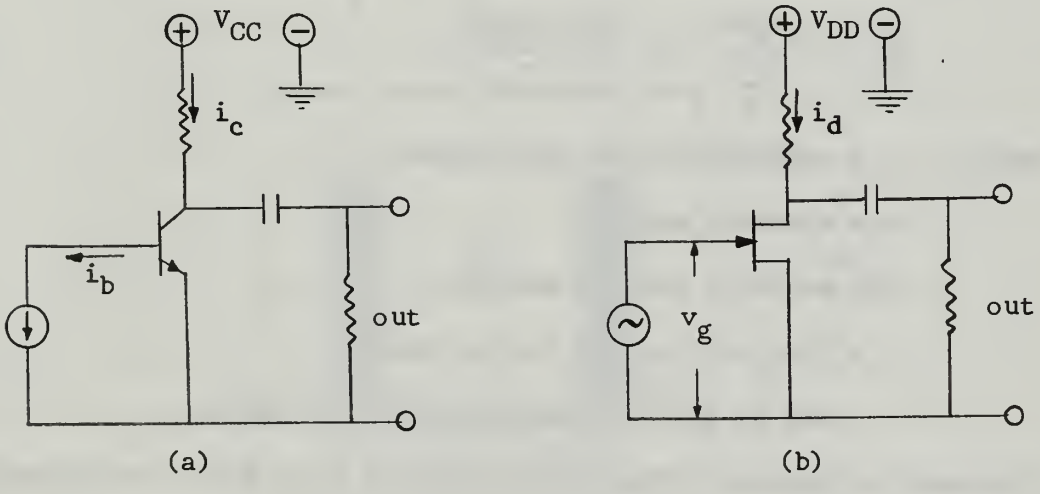

Figure 1. Different methods of current control by using bipolar and unipolar transistors.

(a) i_c is controlled by i_b (with V_{cc} constant)

(b) i_d is controlled by v_g (with V_{DD} constant)

There are two basic types of FETs available at present. These are: (1) junction gate type, and (2) insulated gate type FETs. As explained below, the junction type FETs operate in the depletion mode only, while the insulated gate type FETs have two modes of operation, namely the depletion mode and the enhancement mode.

Since either N (electron conduction) or P (hole conduction) type semiconductors can be used as the current path of the devices, N or P-channel devices can be constructed. The following discussion is based on N-channel devices but also applies to P-channel devices if all polarities are reversed.

The basic junction FET construction and the normal operating bias condition is shown in Fig. 2. Referring to Fig. 2, the approximate channel conductance G_o between source and drain terminal is given by the relation [2]

$$G_o = \frac{\sigma WT}{L} \cong \frac{(q\mu)NWT}{L} \qquad (2\text{-}1)$$

where σ = conductivity of the channel

q = electron charge

μ = majority carrier mobility

N = Electron density in the channel

and W, T, L are as defined in the figure.

The basic principle of the junction FET is to control the effective channel thickness T, and hence the channel conductance, by use of the depletion region formed by the reverse biased P-N junction between gate to source or drain.

A typical output characteristics of a junction FET is shown in Fig. 3.

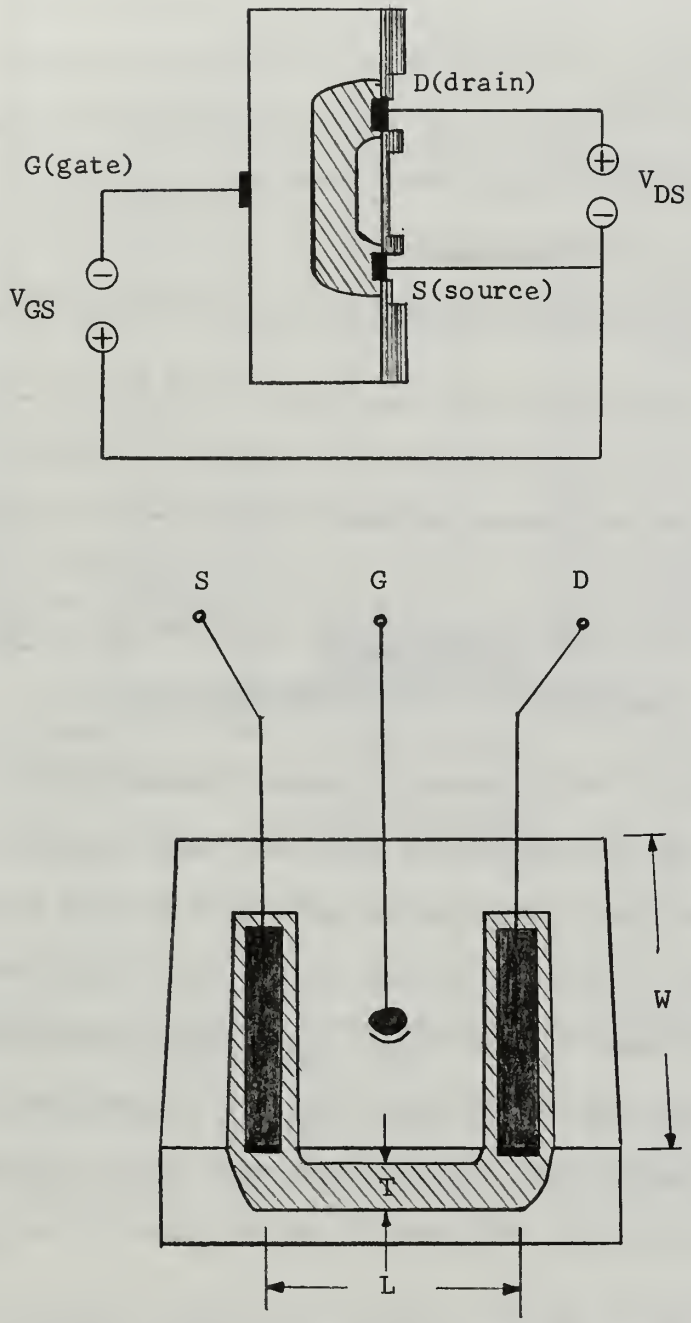

Figure 2. The basic construction of a junction field effect transistor

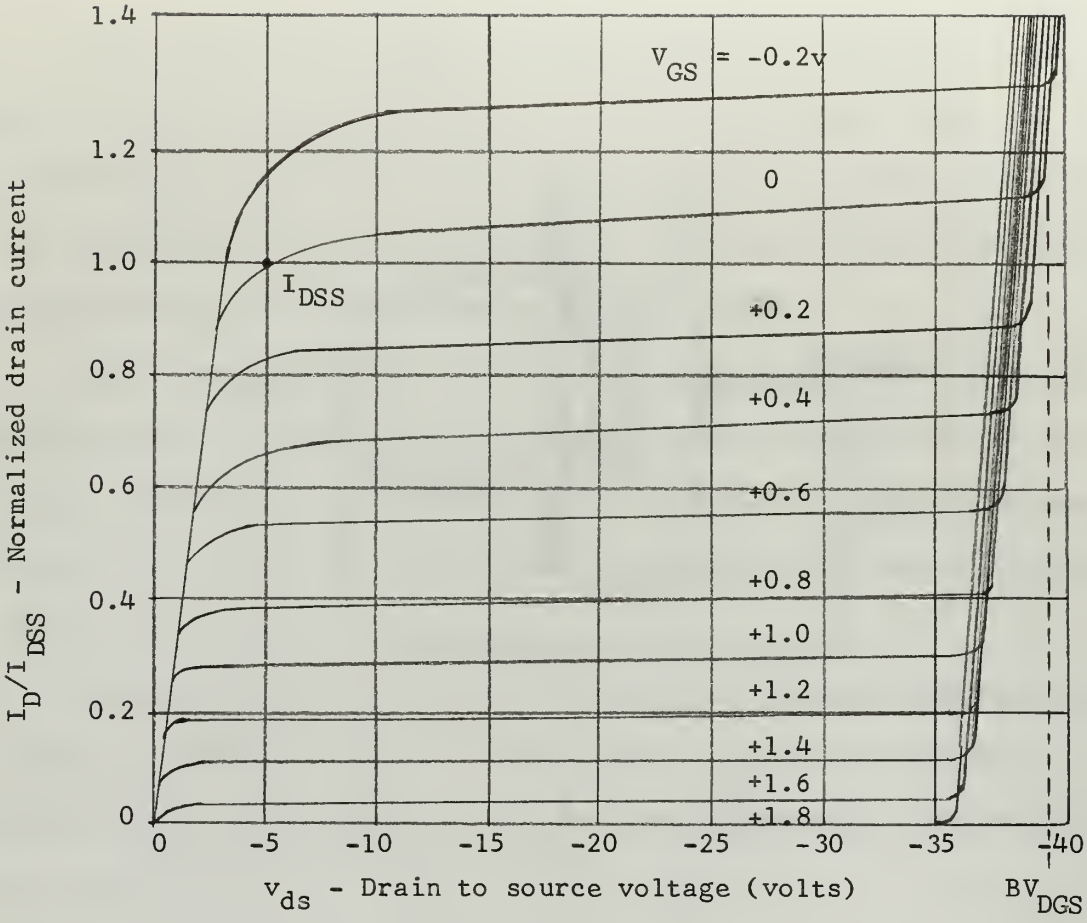

Figure 3. FET I_D versus V_D output characteristics

The terminology and the parameters which are used below are defined in reference 3. They are: drain current with gate shorted to source I_{DSS}, pinch-off voltage V_P, gate-to-source current with drain shorted to source (or drain open) I_{GSS} (or I_{GSO}), breakdown voltages BV_{GSO}, BV_{GDS}, BV_{GSS}, BV_{GDO} and common source forward transconductance g_{fs}.[1]

The other type of FET, the insulated gate type, operates in a similar way but with some difference. As the name of the device im-

[1]The subscripts "S" have different meanings depending on the position in the subscripts. An "S" for the first or second subscript identifies the "source" terminal. An "S" for the third subscript is an abbreviation for "shorted" and indicates that all terminals not designated are tied to the common terminal represented by the second subscript.

plies, the gate electrode is insulated from source, drain and the channel. Therefore, this type of device allows enhancement as well as depletion of the charges in the channel, and permits operation with zero bias, which is impossible in junction FETs. In this paper a particular kind of insulated gate FET, the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is described for the applications in the subsequent sections.

The basic construction of an MOSFET is shown in Fig. 4 in schematic form.

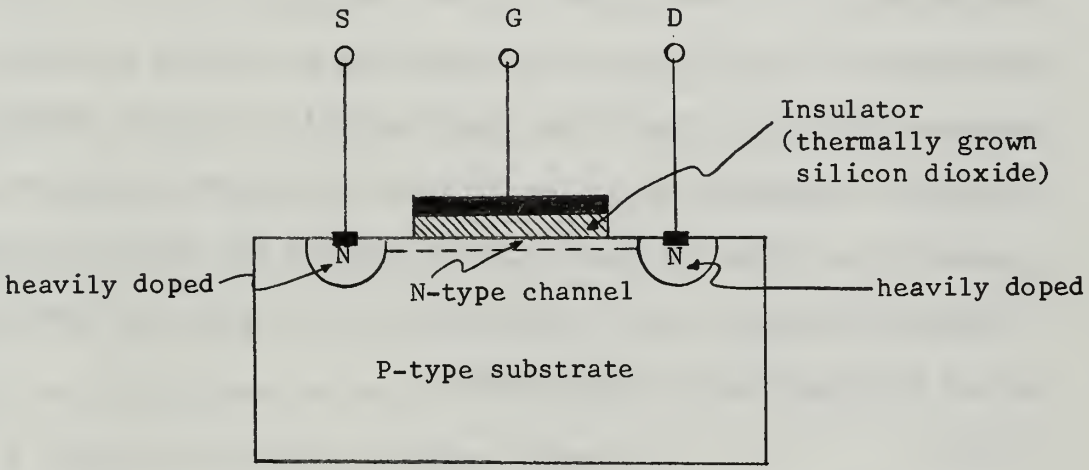

Figure 4. Schematic representation of a MOSFET construction

The degree of the gate electrode coverage of the channel and/or overlapping the source and drain regions varies for different mode type MOSFET. [4]

In the depletion mode, the charge carriers are present in the channel with zero gate bias. Reverse biasing of the gate depletes this charge and reduces the channel conductance. In the enhancement mode the charge carriers are not present in the channel with zero gate bias, and the forward biased gate enhances the channel charge and

increases the channel conductance. Forward (or reverse) biasing of the gate means positive gate potential (or negative gate potential) for an N-channel device as shown in Fig. 4.

Examples of output characteristics for enhancement mode transistors are shown in Fig. 8 and Fig. 13. From these figures and Fig. 4, it can be seen that varied output characteristics are possible merely by changing the doping levels. This property of the enhancement mode FFT enables class-C r-f amplifier operation in a zero bias configuration. The most noticeable features of this device pertinent to the application of r-f power generation are its very high input impedance, typically 10^{12} to 10^{14} ohms, and its gradual saturation switching characteristics. [4] This latter characteristic of present MOSFETs is one of the disadvantages of this device for r-f power generation. As a comparison between the bipolar transistor and the MOSFET saturation voltage, reference 4 gives a typical value of 3 volts for bipolar transistors and about 12 volts for an FET.

Summary

Field effect transistors possess several advantageous properties as mentioned in section one. They also have disadvantageous properties as well, as given in this section. The following sections study some of the pertinent characteristics in connection with class-C or equivalent r-f power amplifier circuits, seeking the best application of the device.

3. Class-C R-F Power Amplifier

High efficiency is extremely important in the r-f power generation stage, not only in economizing on the supplied power but also in permitting large power outputs to be obtained from relatively small devices; both of which the transistor user often desires. These prime objectives of r-f power amplifiers are achieved by operating the device in the class-C mode of operation.

As for conventional vacuum tube class-C r-f amplifiers, class-C operation occurs when the drain current conduction angle is less than 180 degrees. High efficiency in class-C operation is the result of the fact that the drain to source supply voltage V_{DD} supplies energy to the amplifier only when the largest portion of this energy will be absorbed by the tuned circuit at the drain, maintaining a low power dissipation in the device. This relationship can be seen from the oscillograms of class-C r-f amplifier drain voltage, gate voltage and drain current wave forms illustrated in Fig. 5. The basic class-C cmplifier circuit with a parallel tuned load is shown in Fig. 6.

Since there are two types of field effect transistors available, namely the junction types and the insulated-gate field-effect types, both types should be investigated. However, the characteristics of the junction power FETs which were available to the writer revealed that they were not suitable devices for conventional class-C operation. This is due entirely to their operating limitations described below.

The junction FETs operate in the depletion mode only. For normal operation, the gate-source junction is reverse biased. As this junction becomes forward biased, the input impedance drops to a value comparable to ordinary bipolar transistors and the advantage of using FETs as a

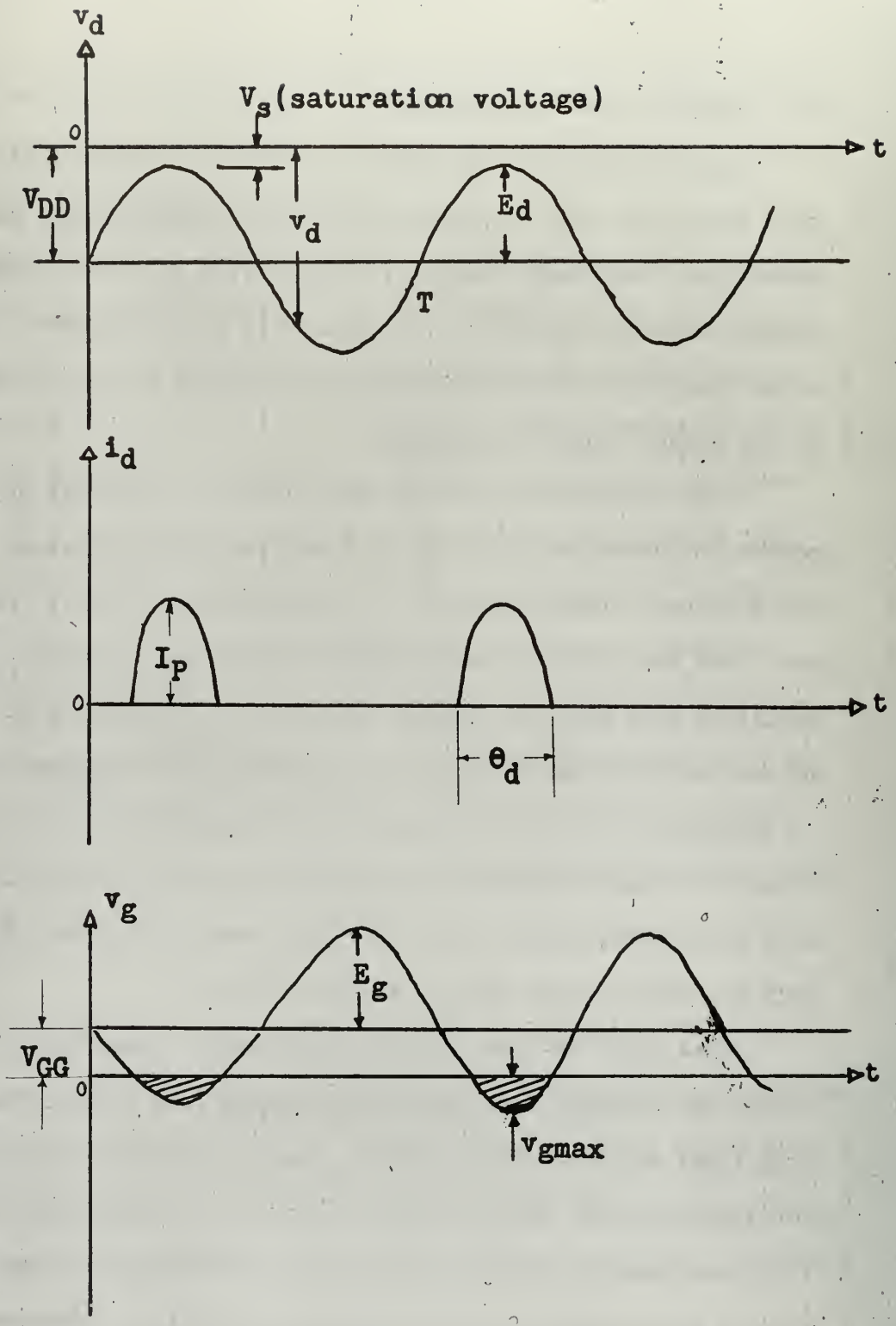

Fig. 5 Class-C r-f Amplifier Drain, Gate Voltages and Drain Current Wave Forms (P-Channel Device)

high input impedance device is lost. Therefore, the gate-to-source voltage swing is limited by the $v_g = 0$ condition in one of the half-cycles of the input excitation voltage.

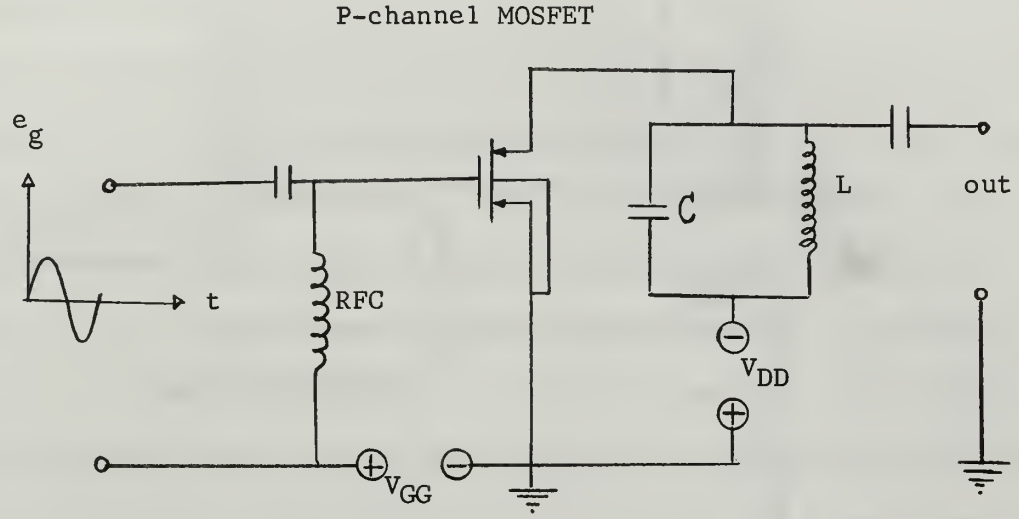

Figure 6. Basic Class-C FET Amplifier Circuit Configuration

The amplitude of the other half-cycle of excitation signal voltage is limited by the gate-to-source reverse breakdown voltage BV_{GS}. For the devices available to the writer, Crystalonics' junction power FETs CP602 and CP603, BV_{GS} was equal to the pinch-off voltage V_P. For class-C operation it is necessary to have BV_{GS} at least greater than V_P. This relation is illustrated in Figure 7. Upon noticing this limitation of these particular junction devices, consideration was given to other general junction FETs. The data for most junction devices found in the manufacturer's specification sheets and technical publications available to the writer, indicated that the difference between the gate-to-source reverse breakdown voltages and the drain current pinch-off voltages were not large enough for class-C operation at reasonably close to ideal conditions; i.e., maximum excitation swing limited by $V_{GS} = 0$ condition.

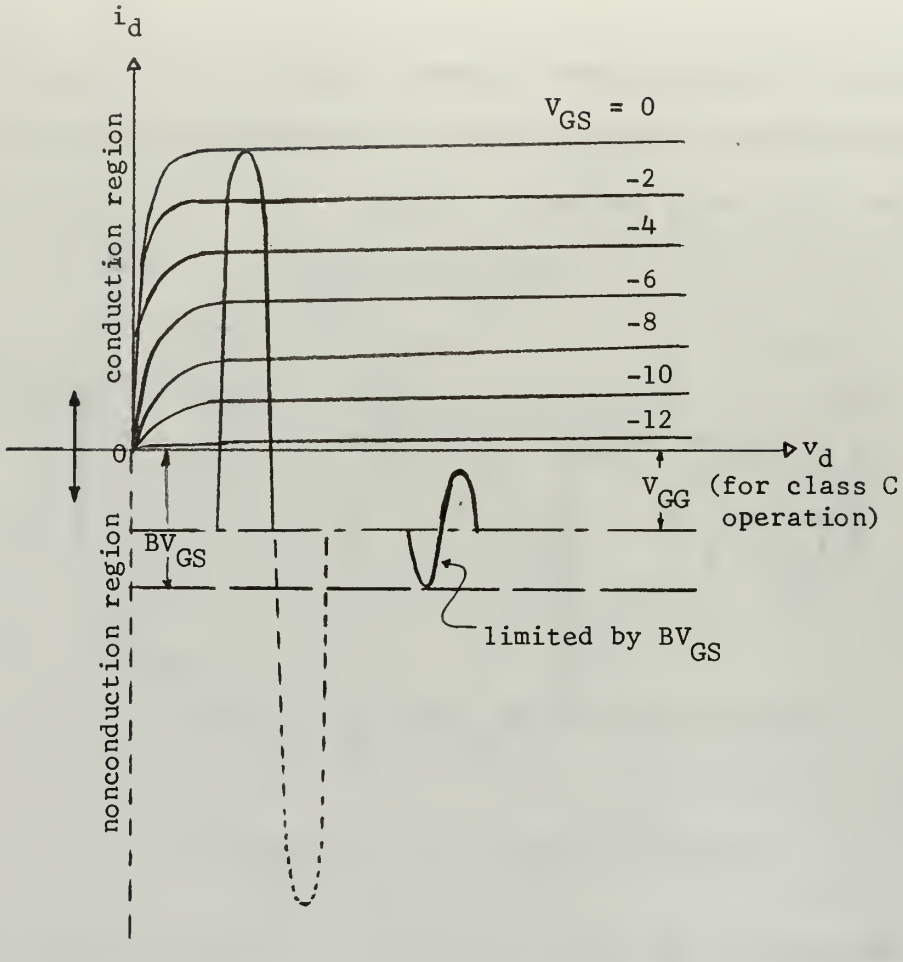

Figure 7. Limitation of Excitation Voltage Amplitude

Since this limitation of junction devices can be removed in the circuit operation described in the next section, and since there are other types of FETs which do not have the limitation mentioned above, the following discussion of FET application to the conventional class-C r-f power amplifier configuration is directed only to the insulated-gate type field-effect transistor. In particular, an enhancement mode MOSFET is used as an example. The reason for this choice will appear in the course of the following discussion.

As with the vacuum tube counterpart, a mathematical analysis of the class-C tuned FET amplifier is complicated and the use of design

charts is a plausible approach. Although this method is only approximate and lengthy, it is directly useful in design since an explicit solution for the optimum operating conditions can be obtained from the semigraphical analysis.

Due to the nonsinusoidal wave form of the varying components of drain current i_d, the path of operating points is not a straight line on the i_d versus v_d characteristic chart, which is the only one supplied by most manufacturers. However, it is shown that the path of operation on the constant current characteristic curves is a straight line for a class-C amplifier with a parallel tuned load. [5] To make use of this advantage, the constant current characteristic curves are plotted from output characteristic curves, Fig. 8, and a few measurements for a positive value of V_{GS}.[1] When the path of operation is superimposed on the constant current curves, the values of the average and fundamental components of the drain current are obtained from the wave form of the drain current. These values are then used to evaluate the amplifier performance.

Since the path of operation is a straight line on the constant current curve, this line can be located by determination of two points. These points are related to the fundamental factors controlling the behavior of class-C amplifiers, i.e., peak drain current during the cycle, saturation voltage V_s, conduction angle θ_d, and drain supply V_{DD}. The leakage current is so small for the MOSFET that it can be neglected in this application.[2]

[1]Positive V_{GS} for N-channel devices and negative V_{GS} for P-channel devices.

[2]For example, I_{GS} = 100 picoamp at V_{GS} = -50 volts, V_{DS} = 0 for FN1034.

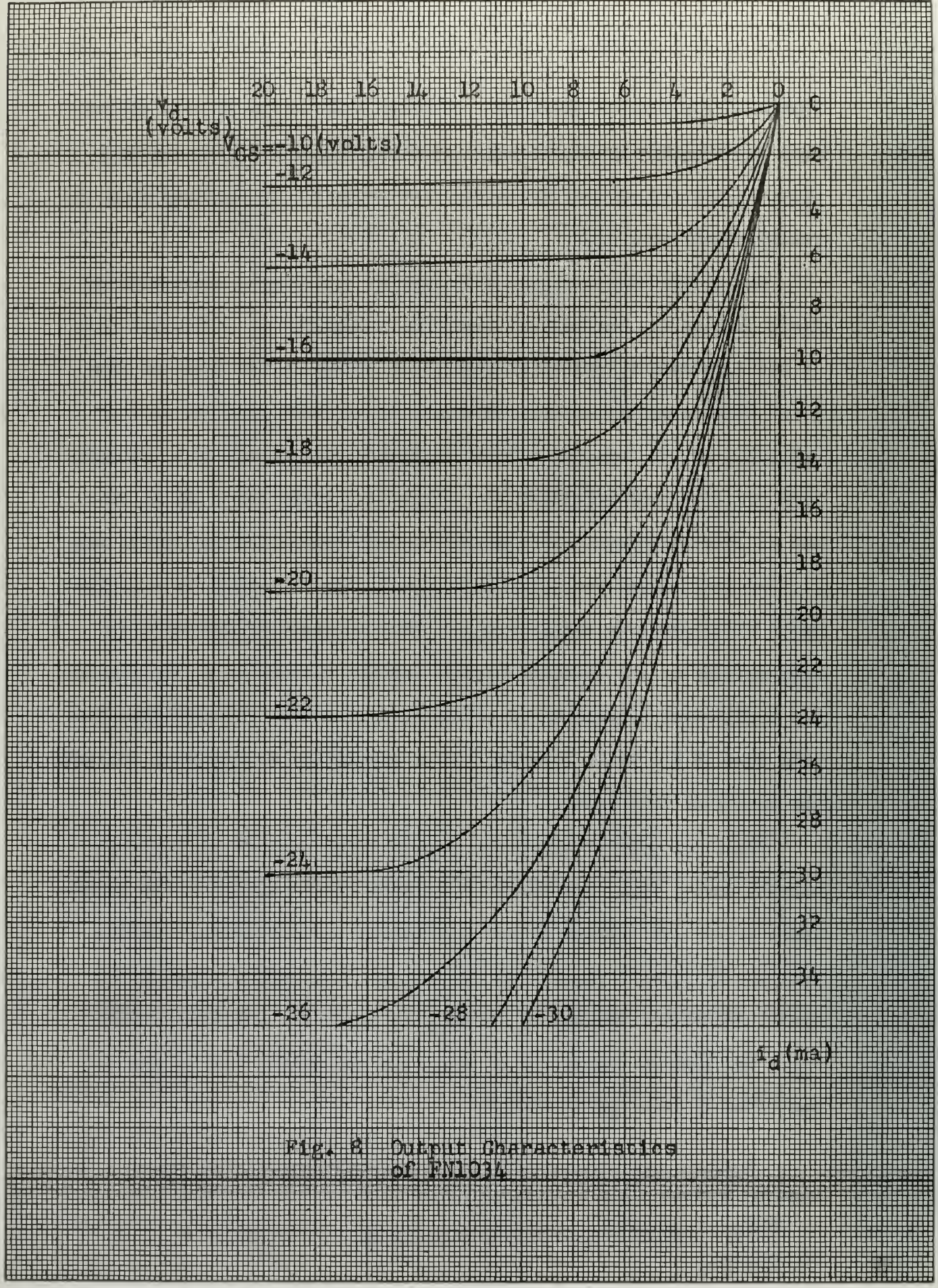

Fig. 8 Output Characteristics of FM1034

The straight-line path of operation in the first and the last quadrant of the cycle is shown in Fig. 9. With ωt equal to zero, the point P is determined by v_{gmax} and V_s. With ωt equal to $\pi/2$, the point Q is determined by V_{GG} and V_{DD}. The distance along the line between the operating point and point Q varies as the cosine of the phase angle in the cycle. Superimposing this operating path on the constant current curves, as shown in Fig. 10, the drain current at particular times in the cycle may be determined.

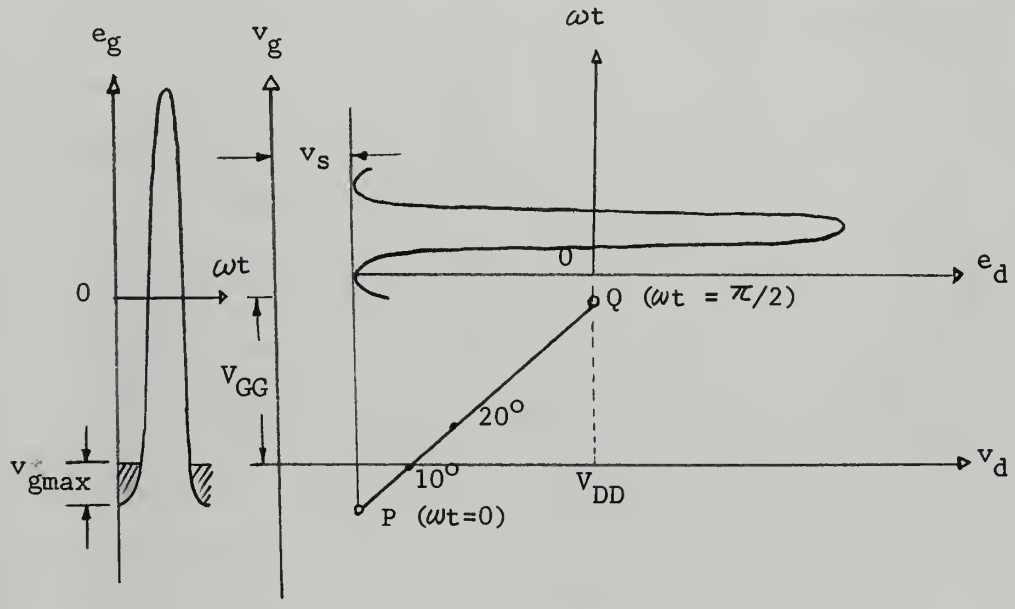

Figure 9. Path of Operation on the v_g vs v_d coordinates

For a systematic analysis of the amplifier performance using a diagram like Fig. 10, the suggested procedures of reference 5 are closely followed. To get specific results from the investigation, an r-f power amplifier stage is analyzed for several operating conditions using an FN1034 P-channel enhancement-mode MOS field-effect transistor. Again, the objective of this analysis is to determine if any of the FET characteristics can advantageously be employed to generate r-f power.

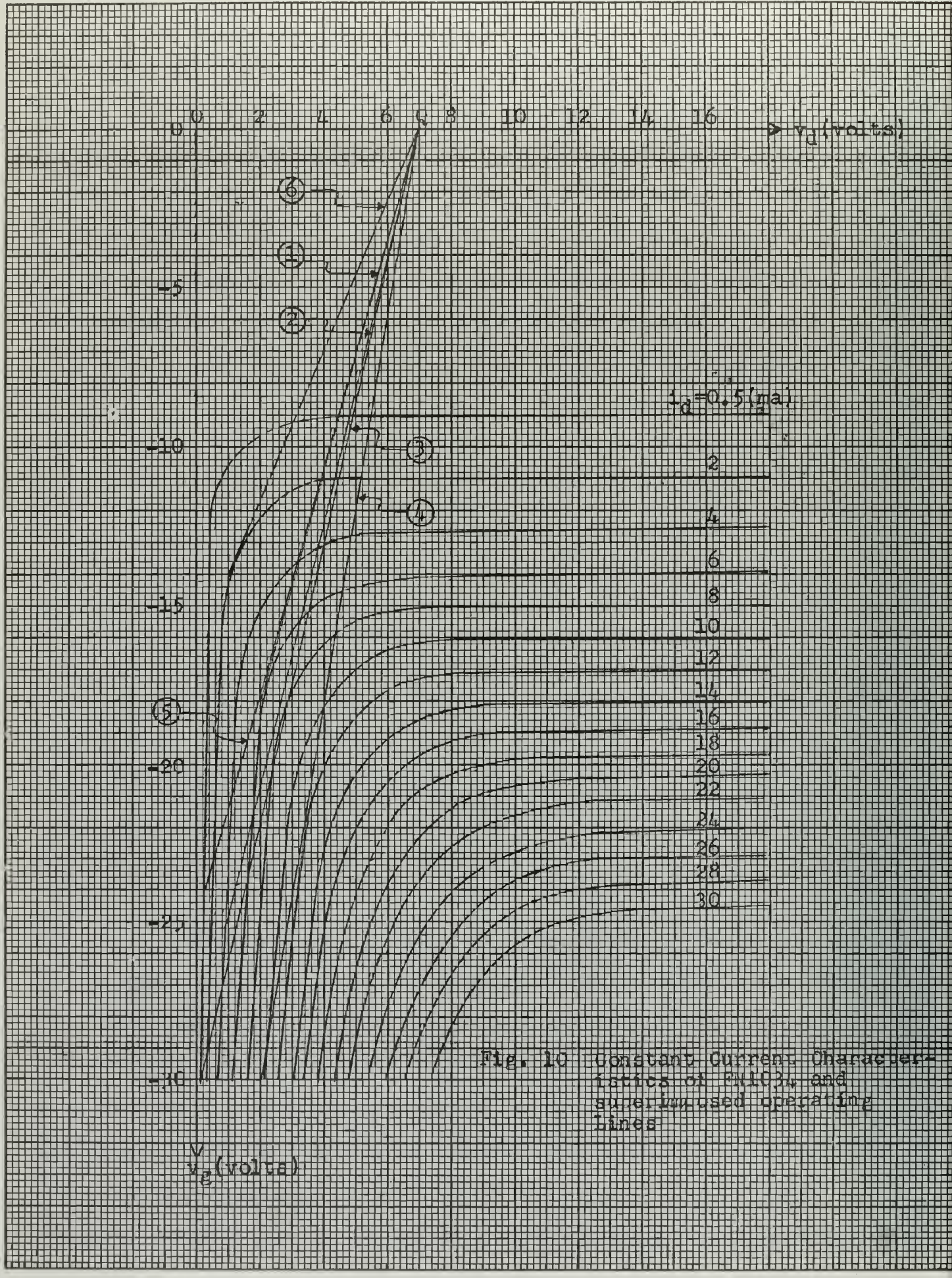

Fig. 10 Constant Current Characteristics of FM1024 and superimposed operating lines

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The illustration shows that by proper choice of the device and the operating conditions, several characteristics can be utilized for this purpose. Also the illustration shows that the device efficiency or the power output can be maximized by proper choice of operating conditions.

For optimum use of the device, maximum safe operating conditions must be considered. The maximum safe drain supply voltage is equal to $BV_{DS}/2$. Maximum safe excitation voltage amplitude E_g is determined by V_{GG}, BV_{GSO} and BV_{GDO}. This relationship is shown in Fig. 11 for the FN1034. With $V_{DD} = BV_{DS}/2 \cong 7$ volts, E_g is determined as follows:
From the BV_{GDO} limiting condition;

$$E_g - |V_{DD}| - |V_{GG}| \leq 50 \qquad \text{or}$$

$$E_g \leq 57 + |V_{GG}| \qquad (3\text{-}1)$$

E_g is also limited by;

$$E_g + |V_{GG}| + |V_{DD}| \leq 12 \qquad \text{or}$$

$$E_g \leq 5 - |V_{GG}| \qquad (3\text{-}2)$$

From the BV_{GSO} limiting condition;

$$E_g + |V_{GG}| \leq 12 \qquad \text{or}$$

$$E_g \leq 12 - |V_{GG}| \qquad (3\text{-}3)$$

and also

$$E_g - |V_{GG}| \leq 50 \qquad \text{or}$$

$$E_g \leq 50 + |V_{GG}| \qquad (3\text{-}4)$$

Referring to the above four relations, it is apparent that very large values of E_g, over 50 volts, may safely be applied to the input terminals if only the positive half cycle of the excitation voltage is

limited to the value given by relations (3-2) or (3-3), whichever is the smaller value of the two. This is permissible since we are using the negative half cycle or less of the excitation voltage to make the device conduct, the device is then cut off during the positive half cycle or more of the excitation voltage. The study of the electrical characteristics of the device shows that the gate excitation power P_{ex} is very small even with an E_g of 50 volts. Using the relation [1]

$$P_{ex} = \frac{E_g I_{g1}}{2} \cong E_g I_{gdc}$$

and the gate leakage current I_{GSB} at V_{GSB} = -50 volts and V_{DSB} = 0 volts,

$$P_{ex} = 50 \times 100 \times 10^{-12}$$

$$= 5 \text{ nanowatts.}$$

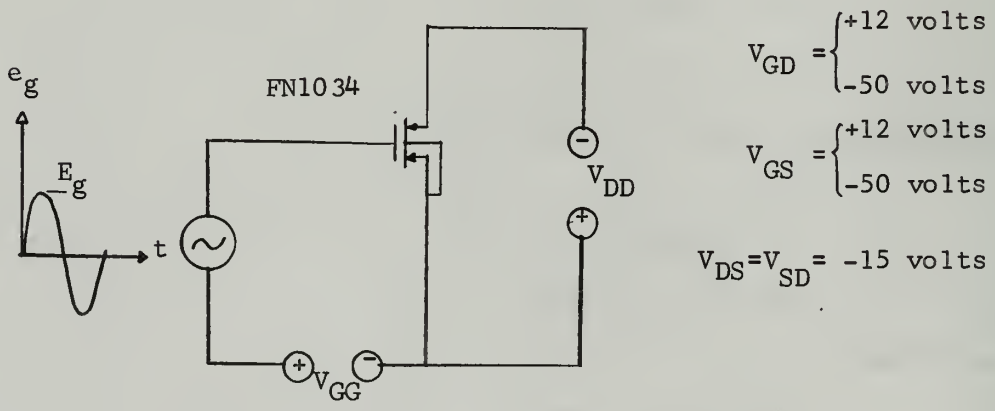

Figure 11. Maximum Safe Operating Conditions for FN1034

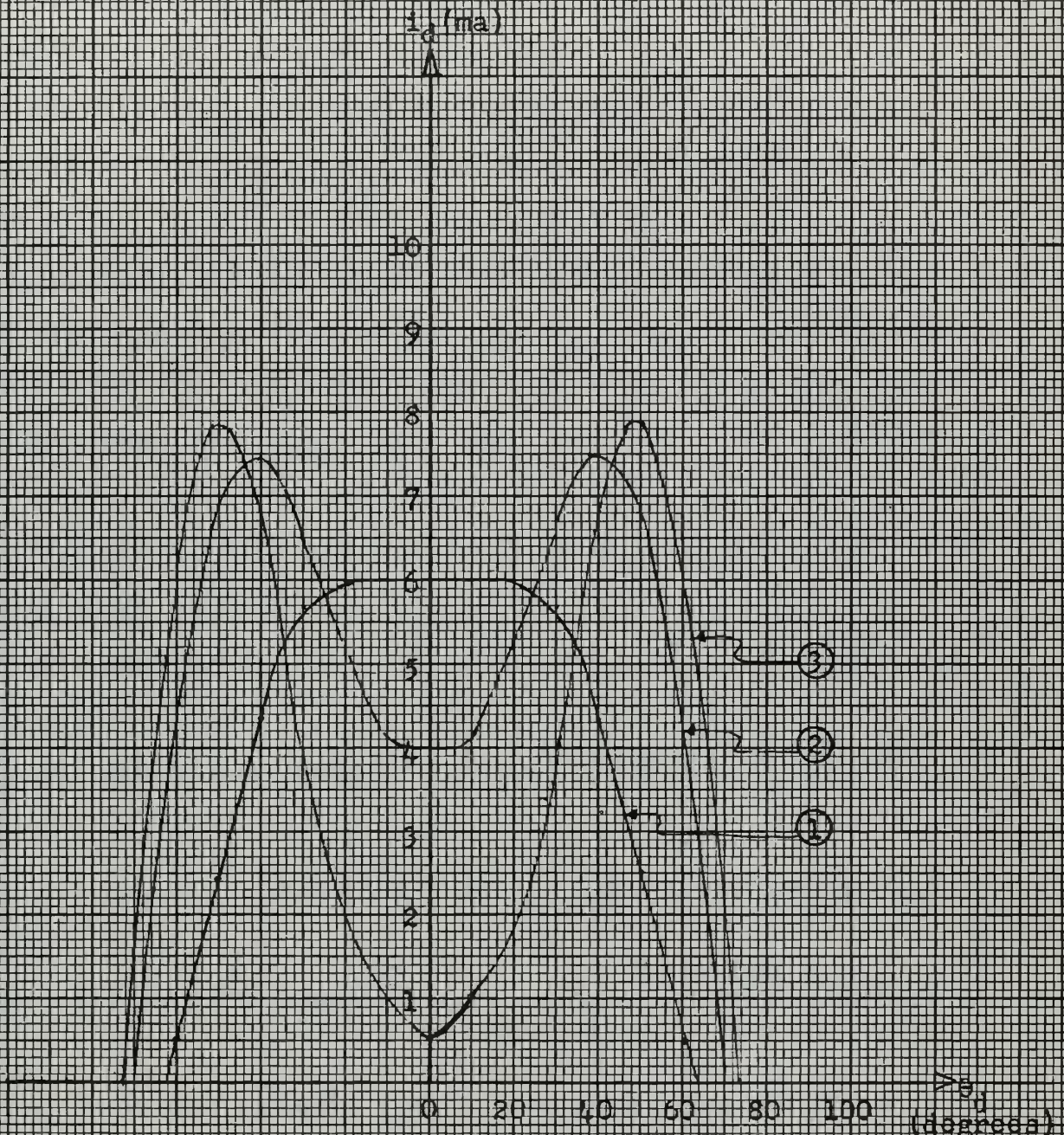

Fig. 12 Output Current Wave Forms for Several Operating Conditions

Table 1. Sample calculation of the amplifier performance. (operating condition ① in Fig. 10)

V_{DD} = 7 volts

E_g = 25 volts

V_{GG} = 0 volts

$v_{gmax} = E_g$ = 25 volts

V_s = 1 volt

i_{dmax} = 7.5 ma

i = 16.4 unit

$n = \pi/\Delta\omega t$ = 18

k = an integer

E_{d1} = 6 volts

1	k	0	1	2	3	4	5	6	7	8	9
2	$\frac{k\pi}{n} \times \frac{360^\circ}{2}$	0	10	20	30	40	50	60	70	80	90
3	$\cos(\frac{k\pi}{n})$	1.0	.985	.940	.866	.766	.643	.500	.342	.174	.000
4	$1\cdot\cos(\frac{k\pi}{n})$	16.4	16.15	15.4	14.2	12.5	10.6	8.20	5.60	2.86	.000
5	$i_d\ (\frac{k\pi}{n})$	4	4.1	5.2	6.5	7.5	6.9	3.6	0.1	0	0
6	$i_d(\frac{k\pi}{n})\cos(\frac{k\pi}{n})$	4	4.04	4.89	5.64	5.75	4.44	1.8	0.034	0	0

$$I_{av} = \frac{1}{n}\left[i_d(0)/2 + \sum_{k=1,2,3\ldots} i_d\left(\frac{k\pi}{n}\right)\right] = 2$$

$$I_{d1} = \frac{2}{n}\left[\frac{i_d(0)\cos(0)}{2} + \sum_{k=1,2,3\ldots} i_d\left(\frac{k\pi}{n}\right)\cos\left(\frac{k\pi}{n}\right)\right] = 3.18$$

$$P_L = \frac{E_{d1} I_{d1}}{2} = 9.54 \text{ mw} \qquad P_{in} = V_{DD} I_{av} = 14 \text{ mw}$$

$$P_d = 14 - 9.54 = 4.46 \text{ mW} \qquad \text{efficiency} = \frac{9.54}{14} = .68$$

Even when the V_{DSB} was increased to -14 volts, the change of I_{GSB} was not detectable with a Simpson 260 meter. This justifies the previous statement that the gate current can be neglected in the approximate semigraphical analysis method employed here.

The value of V_{GG} is chosen by considering the conduction angle θ_d. For example, if $\theta_d = \pi$, or conduction during negative half cycle of the input signal, $V_{GG} = 0$. For non-zero values of V_{GG}, the required value of E_g increases, and for a given value of E_g the output power decreases. In this example $V_{GG} = 0$ was chosen. However, class-C operation was obtained rather than class-B due to the nature of the device characteristics. Since $V_{GG} = 0$; $v_{gmax} = E_g$.

Knowing the maximum safe operating conditions, several operating lines are chosen. These operating lines are drawn in Fig. 10 and several of the resulting drain current wave forms are plotted in Fig. 12. The sample calculation of the amplifier performance at a particular operating condition is given in Table 1 and the results of similar calculations for other operating conditions are given in Table 2.

Table 2. Results of amplifier performance calculated for different operating conditions.

Operating line in Fig. 10	E_g (volts)	V_s (volts)	P_{in} (mw)	P_L (mw)	efficiency	remarks
1	18	2	10.9	6.85	0.63	
3	30	0.3	11.6	7.75	0.67	
4	30	2	26.4	15	0.57	large output power
5	24	0.3	8.25	5.87	0.71	
6	14	1	3.3	2.53	0.77	high efficiency

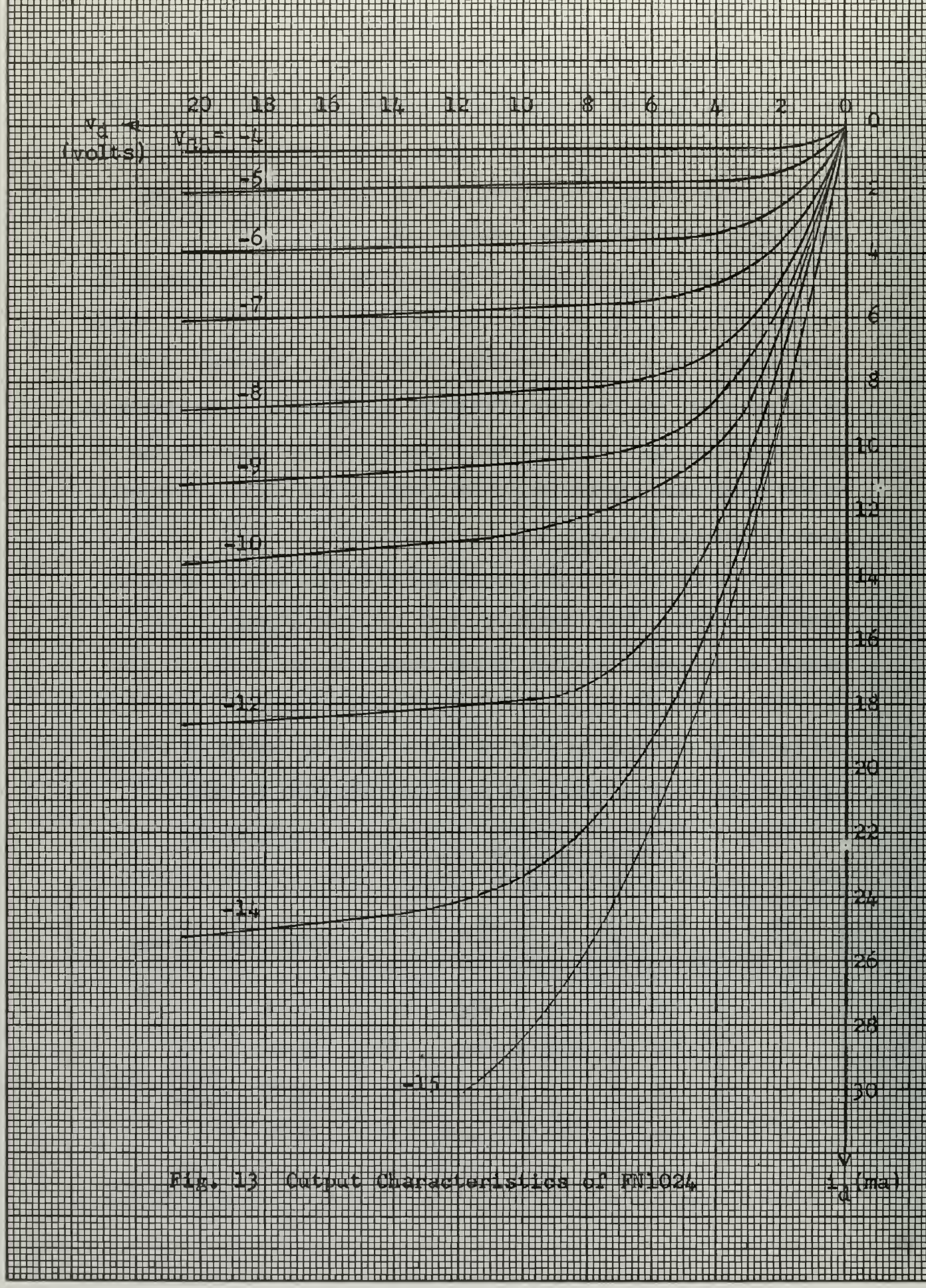

Fig. 13 Output Characteristics of FN1024

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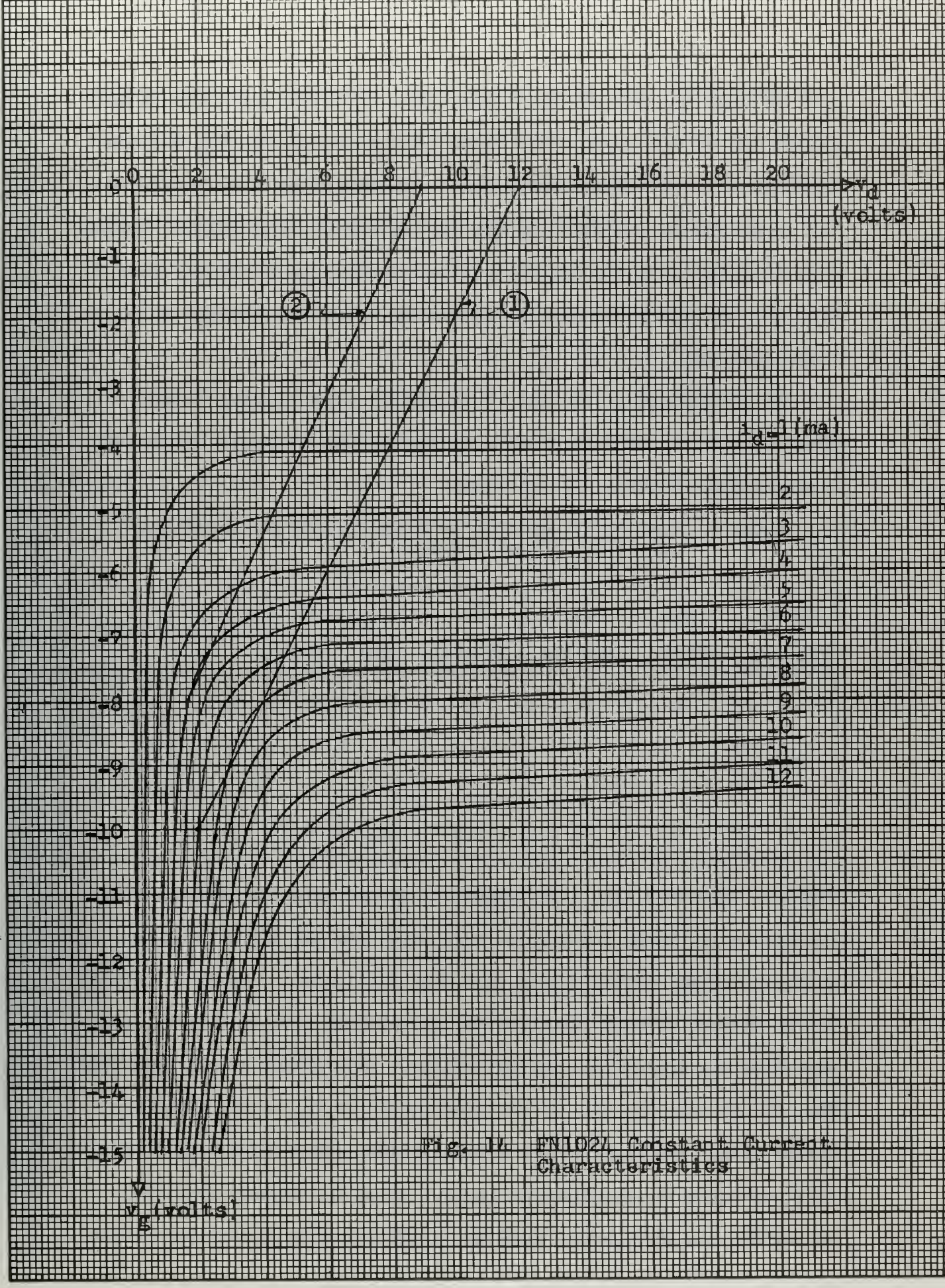


Fig. 14. EN102A, Constant Current Characteristics

To show that the choice of the device is important both for high efficiency and for large output power, a similar device with somewhat different characteristics was chosen. The output characteristics of the chosen device are shown in Fig. 13 and the constant current characteristic curves with two operating lines superimposed on it are shown in Fig. 14. Following the same procedures as before the results in Table 3 are obtained.

An examination of the two illustrations above reveals several advantages of the MOSFETs as well as some of the drawbacks for use in a conventional class-C r-f amplifier.

Table 3. Results of amplifier performance for two operating conditions chosen (FN1024)

number in Fig. 14	V_{DD} (volts)	E_g (volts)	V_s (volts)	P_{in} (mw)	P_L (mw)	Eff.	Remarks
1	12	10	2	19.7	16.6	.845	High eff. decreased Miller effect Voltage gain = 1
2	9	8	1.6	10.2	7.2	.71	

From the extremely high input impedance characteristics of the MOSFET, the excitation power required is very small and the driver stage can be a simple voltage output device with very small power. By proper choice of the device, class-C operation can be achieved without biasing, thus enhancing the overall circuit efficiency. This effect can be seen from Fig. 10, 12 and Fig. 14. Proper combination of V_{DD} and E_g reduces Miller effect for high frequency application, since voltage gain under this condition is approximately unity. Among the drawbacks of this device are its small power handling capability with present production

MOSFETs and requirement for a high excitation voltage. The disadvantage of a high excitation voltage requirement can easily be solved by employing a tuned input circuit. This scheme is possible due to the high input impedance characteristic of the MOSFET.

4. Pulse-Excited R-F Power Amplifier Circuit

It was mentioned in the foregoing section that the junction field effect transistors are not suitable devices for conventional class-C r-f power amplifier circuits. The main reason for this is the inherent operating limits of the junction FET. These limits, however, can be eliminated if the device is used in a pulse-excited switching-mode r-f amplifier circuit. Again the gate biasing is not necessary but the problem of generating asymmetrical excitation pulses arises. In the following study, the operating performance and the design considerations of the pulse-excited r-f amplifier stage are discussed. At the end of section, a design example is given using a Crystalonics' power field effect transistor CP603.

A typical parallel tuned circuit configuration is shown in Fig. 15.

N-channel FET

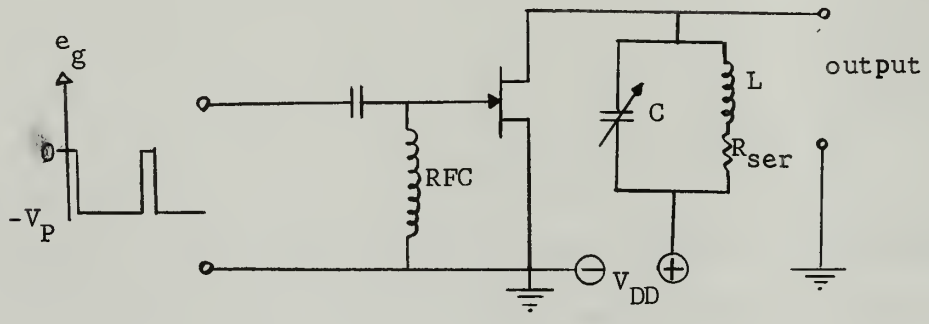


Figure 15. Basic tuned Amplifier Circuit

The tuned circuit connected in the drain circuit of the device is very seldom, if ever, a simple parallel arrangement such as shown in Fig. 15. For proper operation of the device the required impedance at the device output terminals is fixed, and the actual load impedance is generally also fixed by external load conditions. Although a more com-

plicated circuit is connected to the device output terminals to perform necessary impedance transformations mentioned above, the coupling network and load can usually be reduced to an equivalent simple parallel tuned circuit at a particular frequency. In Fig. 15, R_{ser} includes the coupled resistance from the actual load.

The loaded Q, Q_L, of the drain tank circuit, $\omega_o L/R_{ser}$, should be high enough to provide reasonable discrimination against the harmonic components contained in the drain current pulses. In practice, Q_L of 10 represents a typical value [1]. At the same time, the input impedance of the drain tank circuit must meet the device operating condition,

$$R_t = \frac{E_{d1}}{I_{d1}} \tag{4-1}$$

where R_t is the impedance at resonance, E_{d1} and I_{d1} are the amplitudes of the fundamental components of the drain voltage and current. E_{d1} and I_{d1} will be determined in the subsequent development. This value of input impedance is related to the drain tank circuit components values and Q_L by the relation [5]

$$R_t = Q_L\sqrt{\frac{L}{C}} = \frac{L}{R_{ser}C} = \frac{(\omega_o L)^2}{R_{ser}} \tag{4-2}$$

From these relations, the value of the input impedance required by the device can be obtained by simultaneous selection of Q_L and the L/C ratio of the tank circuit.

For the determination of E_{d1} and I_{d1}, and the evaluation of the performance of the circuit, the gate input voltage, drain current and drain voltage wave forms shown in Fig. 16 will be used.

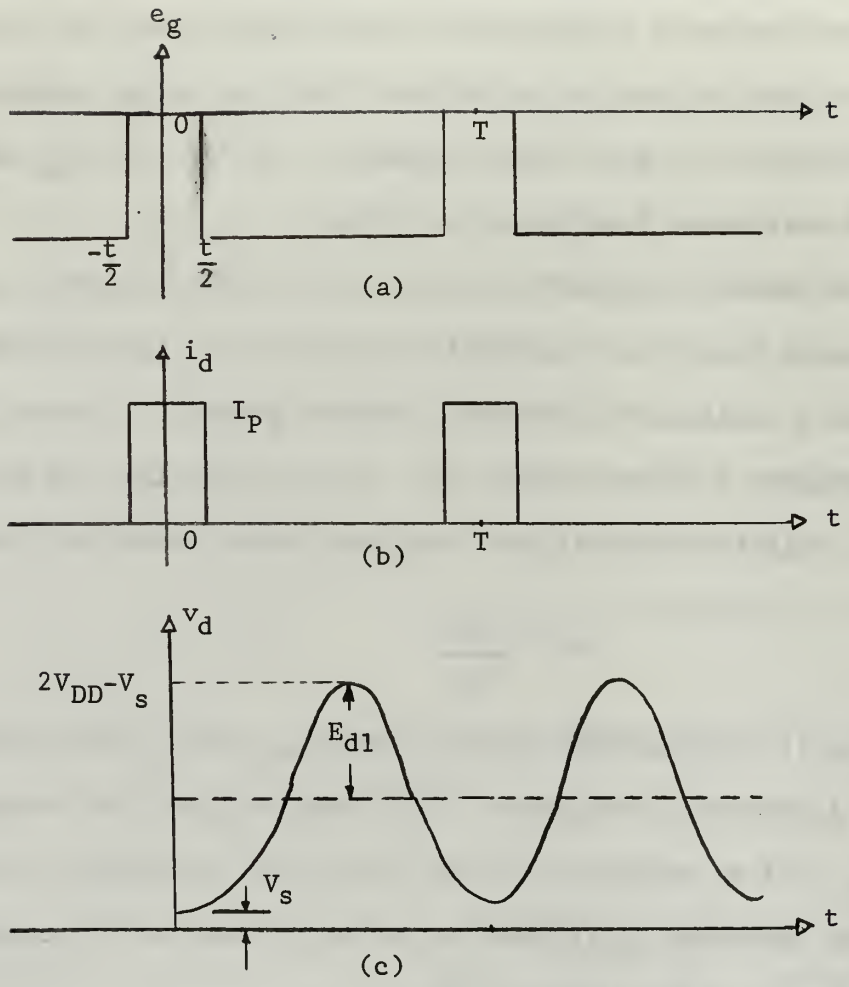


Figure 16. Gate Voltage (a), Drain Current (b) and Drain Voltage (c) Wave Forms

The value of I_p is obtained from the manufacturer's specification sheets. The average value of the drain current, I, is given by:

$$I = \frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} i_d \, dt$$

$$= \frac{1}{T}\int_{-\frac{t_o}{2}}^{\frac{t_o}{2}} I_p \, dt$$

$$= \frac{I_p}{T} t_o \qquad (4\text{-}3)$$

where T is the period of input pulse and t_o is the conduction time. The amplitude of the fundamental component of the drain current, I_{d1}, is obtained from the relation:

$$I_{d1} = \frac{2}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} i_d \cos\frac{2\pi}{T}t\, dt$$

$$= \frac{2}{T}\int_{-\frac{t_o}{2}}^{\frac{t_o}{2}} I_p \cos\frac{2\pi}{T}t\, dt$$

$$= \frac{2I_p}{\pi}\sin\frac{\pi}{T}t_o \qquad (4\text{-}4)$$

The amplitude of the fundamental component of alternating drain voltage E_{d1} is:

$$E_{d1} = \left|V_{DD}\right| - V_s \qquad (4\text{-}5)$$

where V_s is the saturation voltage across the device during maximum current conduction and is dependent upon the value of saturation resistance of the device at a particular I_p. Substituting equations (4-4) and (4-5) into equation (4-1), the load impedance required for the device operating conditions is obtained in terms of known quantities.

$$R_t = \frac{E_{d1}}{I_{d1}}$$

$$= \frac{V_{DD} - V_S}{\frac{2I_p}{\pi}\sin\frac{\pi}{T}t_o}$$ or

$$R_t = \frac{\pi (V_{DD} - V_S)}{2 I_p \sin \frac{\pi}{T} t_o} \qquad (4\text{-}6)$$

To evaluate the performance of the circuit, the drain efficiency is examined. By definition the drain efficiency is given by:

$$\text{Drain eff.} = \frac{P_L}{P_{in}}$$

where P_{in} is the dc power supplied to the drain circuit and P_L is the ac power output.

$$P_{in} = V_{DD}\, I$$

Substituting equation (4-3) into the above relation:

$$P_{in} = \frac{t_o}{T} V_{DD}\, I_p \qquad (4\text{-}7)$$

Output power is given by:

$$P_L = P_{in} - P_d$$

where P_d is the power dissipated in the device and is computed by the relation:

$$P_d = \frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} v_d\, i_d\, dt$$

$$= \frac{1}{T}\int_{-\frac{t_o}{2}}^{\frac{t_o}{2}} I_p \left[V_{DD} - (V_{DD} - V_S)\cos\frac{2\pi}{T} t\right] dt$$

$$= \frac{I_p}{T}\left[V_{DD} t_o - \frac{T}{\pi}(V_{DD} - V_S)\sin\frac{\pi}{T} t_o\right] \qquad (4\text{-}8)$$

$$P_L = \frac{I_P}{\pi}(V_{DD}-V_S)\sin\frac{\pi}{T}t_o \qquad (4\text{-}9)$$

Therefore the drain efficiency is:

$$\text{drain eff.} = \frac{\frac{I_P}{\pi}(V_{DD}-V_S)\sin\frac{\pi}{T}t_o}{V_{DD}I_P\frac{t_o}{T}}$$

$$= \frac{T(V_{DD}-V_S)}{\pi V_{DD}t_o}\sin\frac{\pi}{T}t_o \qquad (4\text{-}10)$$

From equation (4-10), it is seen that the smaller the value of t_o the higher the drain efficiency. Also the drain efficiency is dependent upon the saturation voltage across the device. Hence, a device having small V_s is desirable for this type of operation.

To illustrate the foregoing discussion a circuit example will be given along with design procedures.

Assume that an r-f power source of about 200 milliwatts output to a 220 ohm load at an operating frequency of 500 kc is to be designed using an FET. As mentioned at the beginning of this section, the load to which the specified a-c power is to be delivered is thus fixed. Since the drain tank circuit impedance required for the proper operation of the circuit is also fixed by equation (4-6), the drain tank circuit including the specified load must satisfy relation (4-6) and at the same time optimum power must be delivered to the actual load with minimum dissipation in the intermediate connecting circuitry. For a first approximation, assume that the coupling circuit efficiency can be made

very high. This assumption is reasonable since our load is reasonably large compared to loss resistances associated with the L and C coupling network. From equation (4-9)

$$P_L = (V_{DD} - V_s) \sin \frac{\pi}{T} t_o$$

Choosing a conduction angle of $\pi/2$ or $t_o = T/4$,

$$P_L = (V_{DD} - V_s) \frac{1}{\sqrt{2}} \qquad \text{or}$$

$$\sqrt{2}\,\pi P_L = I_P (V_{DD} - V_s) \qquad (4\text{-}11)$$

Any device which can satisfy equation (4-11) will meet the requirements. In this example, however, the FET in hand, which is a Crystalonics' CP603 junction power FET is used. The I_P given in the specification sheet is 180 milliamperes at $V_{GS} = 0$, $V_{DS} = 5$ volts $= V_s$. Without further calculation, we can immediately see that this device will give poor efficiency because of its comparatively large saturation voltage. Again referring to the absolute maximum ratings in the specification sheet, $V_{DD} = 10$ volts will give the required output power. A drain efficiency of about 50% can be expected, which is very poor. If, instead of a CP603, we could find a device which has a lower value of V_s, for instance, $V_s = 0.5$ volts, the drain efficiency would be about 86% as determined from equation (4-10).

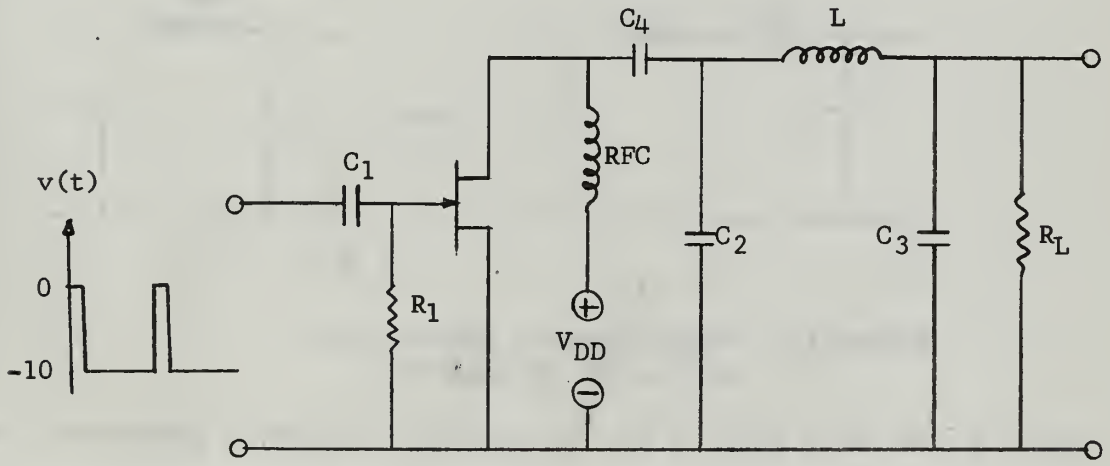
The load impedance required for the device operating conditions at the desired resonant frequency is obtained from equation (4-6).

$$R_t = \frac{\pi (V_{DD} - V_S)}{2 I_P \sin \frac{\pi}{T} t_o}$$

$$= \frac{3.14 \times 15}{2 \times 180 \times 10^{-3} \times 1.4142}$$

$$\cong 33 \ \Omega$$

Since this required tank circuit impedance at the operating frequency is very low compared to the external load, an ordinary parallel tank circuit with impedance transforming, used in the conventional high output impedance circuits cannot be used. However, as can be seen from the relation (4-6), R_t depends on $(V_{DD} - V_s)$ and I_P with t_o fixed. When this relation gives a very high R_t compared to the external load, an ordinary parallel tank circuit can be used. In this illustrative example R_t is less than the actual load and therefore another impedance transforming circuit shown in Fig. 17 will be used.



Component values: capacitors in microfarads

C_1 = .02	C_3 = .0376
R_1 = 22 megohm	R_L = 220 ohm
RFC = 3 mh; .7 ohm	V_{DD} = 10 volts
L = 3.74 microhenry	C_2 = .0965

Figure 17. Circuit for design example

This π-coupling network is adjusted to transform, at the operating resonant frequency, the 220 ohm load to 33 ohm as required to match the impedance of the device. This particular coupling network has the advantage of better harmonic suppression characteristics due to the shunt-capacitive arms. The design procedures for this impedance transforming network are found in many standard text books. Essentially this π-network is considered as two back-to-back L-networks and after calculating the input and output L section of the π-network, the series elements are combined to give a π-network. This equivalent relation of the L and π-network is shown in Fig. 18.

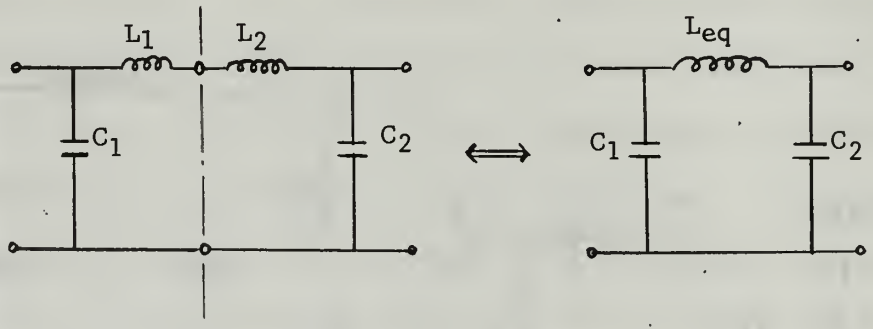


Figure 18. Back-to-back L network and equivalent π-network

Choosing the value of Q_L = 10, for reasonable harmonic suppression and relatively low losses in the L-C circuit, the π-network component values at the operating frequency are computed according to the procedures given in the reference. [8]

The efficiency of this amplifier is limited primarily by the large saturation resistance of the FET. Compared to conventional bipolar transistors, switching FETs were found to have very large saturation resistance. Since this resistance is an inherent device characteristic and the power dissipated in it cannot be avoided, the device efficiency in this application is very low when compared with bipolar transistors.

Therefore, consideration is now given, in the following section, to another use of FETs for solving the problem of efficient r-f power generation.

5. Hybrid Circuit Application

It was found, in the previous two sections, that FETs in their present state of development are inferior to conventional bipolar transistors for r-f power generation as far as device efficiencies are concerned. However, as in the many other circuit applications, field effect transistors can provide advantages over bipolar transistors used alone, when FETs and bipolar transistors are used in combination. In this way certain superior characteristics of one type to the other may be selectively employed in a combined circuit operation. One FET application of this nature is investigated in this section.

Ordinary bipolar switching transistors provide far better device efficiency than present switching FETs, and the power handling capability is also better, at least at present status of device manufacturing and circuit design. It can therefore be concluded that an FET r-f power generator is inferior to the bipolar transistor counterpart as far as its efficiency and power handling capability are concerned. However, with the bipolar transistor alone, one of the r-f power generation circuit design objectives of low excitation power requirement is missing due to the inherent low input impedance characteristics of bipolar transistors, unless some other compensating scheme is employed.

For the compensation of this disadvantage, a high input impedance field-effect transistor can be used in the input circuit of conventional device r-f power generator in such a way that the input impedance of the whole stage is high. To justify and illustrate the above statements, an actual working circuit model is given below with laboratory test results.

The final amplifier stage used here is the series-tuned switching-

mode transistor r-f power amplifier circuit developed by Dr. Ewing in reference 7. This circuit is chosen since it gives the highest possible efficiency among many other existing circuits. This circuit arrangement is reproduced in Fig. 19.

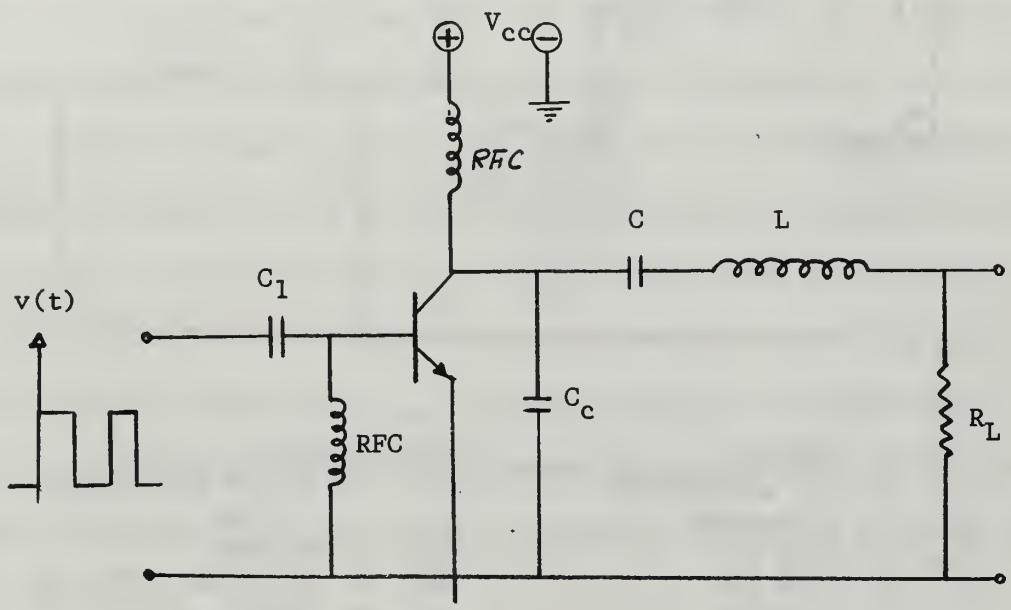
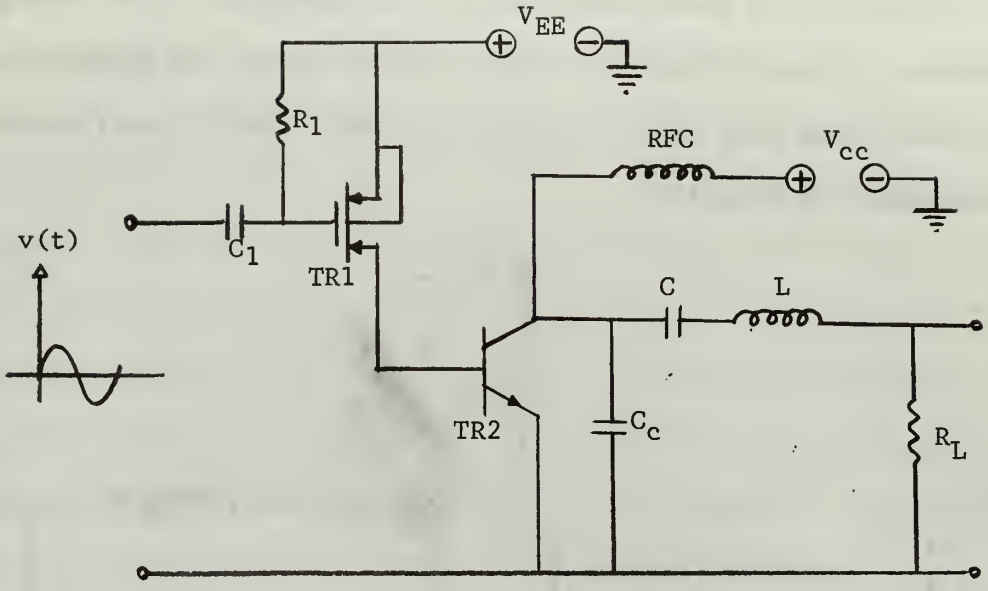


Figure 19. High Efficiency R-F Power Amplifier Circuit Configuration (Reproduced from Reference 7)

The extremely high collector efficiency provided by this circuit configuration may be combined with a very high input impedance FET excitation stage which requires very low excitation power thereby increasing the power gain and the overall efficiency. The illustrative circuit model with its component values is shown in Fig. 20. These component values are obtained from calculations using the design formulas and detailed adjustment procedures given in the reference. The FET in the input circuit is chosen by considering the following required and preferred conditions.



TR1	=	FN1024	TR2	=	2N697
C_1	=	.02 microfarad	L	=	30 58 microhenry
R_1	=	22 megohm			.36 ohm
C_c	=	1360 pf	R_L	=	27 ohm
C	=	3035 pf	RFC	=	3.053 mh; .686 ohm
V_{EE}	=	8 volts	f	=	500 kc
			V_{cc}	=	8 volts

Figure 20. Illustrative hybrid circuit model

For this circuit to be excited by a sinusoidal input voltage, which is the most easily obtained wave form, the transistor TR1 should be an enhancement mode FET, preferably one which has high transconductance g_{fs} and has output characteristics giving a steep-edged drain current wave form of about 180 degrees of the input signal cycle. [7] The current rating of TR1 must be large enough so that it can provide TR2 with sufficient base current to achieve saturation. The reverse breakdown voltage and transconductance must also be large to give this current saturation condition. For this particular circuit configuration shown in Fig. 20 , TR1 must be a P-channel device.

The selection of TR2 was done primarily in accordance with the

conditions specified in the reference. In addition to these critical operating conditions required by TR2, it is desirable to have a high β for higher overall dc to ac power conversion efficiency of the stage.

The above mentioned criteria are met for both transistors used by the author; a P-channel enhancement mode MOSFET FN1024, and a 2N697 NPN switching transistor. This circuit was built and tested in the laboratory. Figure 21 shows an oscillogram taken from an oscilloscope type AN/USM-140 equipped with a dual trace feature having 10 megohm-10 picofarad probes. From this figure, the peak load voltage V_L is found to be 6 volts. The peak collector voltage across TR2 is 22 volts which is well below the measured BV_{CE} of about 35 volts. The measured dc current with 8 volts V_{CC} was 90 milliamperes, giving the total dc input power of 720 milliwatts. The power dissipated in the RFC is given by

$$P_{RFC} = (90 \times 10^{-3})^2 \times 0.686$$

$$= 5.55 \text{ milliwatts.}$$

Therefore, the actual input power to the collector circuit is 714.5 milliwatts. The peak load current I_L is

$$I_L = \frac{6}{27} = 0.222 \text{ amperes.}$$

The ac power delivered to the load P_L is

$$P_L = \frac{V_L I_L}{2} = \frac{6 \times 222}{2} = 666 \text{ milliwatts}$$

$-v_L$ = 5 volts/division; .5 microseconds/division

v_c = 10 volts/division; .5 microseconds/division

Figure 21. Oscillogram of Inverted Load Voltage $-v_L$ and Collector Voltage v_c

Neglecting the power lost in the distributed resistance of inductor L and the capacitor C, the collector efficiency of the amplifier is calculated to be approximately

$$\text{eff.} = \frac{666}{714.5} = 0.932 \quad \text{or} \quad 93.2\%$$

To see the advantage of the MOSFET in the input circuit, the excitation voltage and current were monitored. An HP 650-A test oscillator was used as a sinusoidal source. The peak excitation voltage E_g was 9 volts and the dc gate current flowing would not deflect a 100 microampere full scale ammeter, therefore the excitation power is negligibly small compared to the output power. This very high input impedance excitation stage suggests the possibility of using a tuned input circuit configuration as was mentioned in section three. The dc power supplied to the FET was 4 ma. at 8 volts or 32 milliwatts. Therefore the overall stage dc-to-ac conversion efficiency is approximately

$$\text{eff.} = \frac{666}{720 + 32} = 0.885 \text{ or } 88.5\ \%.$$

This overall efficiency can be further improved by proper choice of devices, TR1 and TR2, and circuit component values. Among other things, the ratio of saturation resistance of TR2 to load resistance must be kept small.[7] In this illustrative circuit the measured saturation resistance of TR2 was 9 ohm at an I_p of 200 milliamperes. There are many switching transistors commercially available today which have saturation resistances, at the same I_p, of a fraction of an ohm. This effect of the relatively large R_s of this illustrative circuit appears in the oscillogram of Fig. 21 as a noticeable voltage drop across the transistor during the conduction period of the signal cycle.

If a larger β transistor is selected for TR2, a lower current rating FET can be used which, at the same time, promotes overall stage efficiency.

The circuit can be operated by a single voltage power supply. Figure 22 shows this single voltage power supply hybrid circuit example.

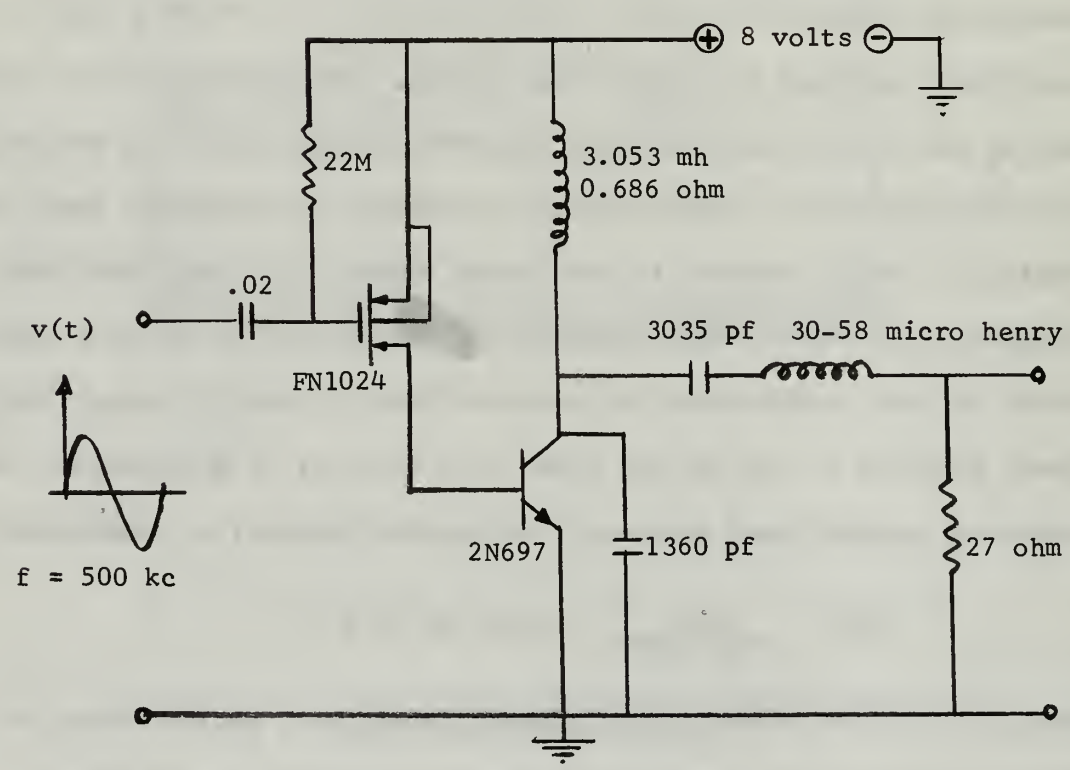


Figure 22. Single Power Supply Hybrid R-F Power Generator

The performance of this circuit is as given previously.

6. Conclusions

Although the unipolar field effect transistors possess several advantages over conventional bipolar transistors, this study reveals that when used alone as an r-f power device, FETs are inferior to the conventional transistors as far as the device efficiency is concerned. This conclusion is based on the study of publications available to the writer and some case studies of applications of the devices. It should also be mentioned that the above statement applies to the present status of device manufacturing and design technique.

The low drain efficiency is primarily due to the large saturation resistance and hence the saturation voltage. Another weak point of FETs as compared to standard transistors are their low power handling capability. At present bipolar transistors far exceed the capability of FETs in power handling ability.

Notwithstanding these disadvantages, the case studies show several advantages in certain applications. The enhancement MOSFETs can provide class C operation without biasing. The excitation power to an MOSFET power amplifier is extremely small and could be operated from a tuned input circuit.

The most advantageous use of FETs to r-f power generation, which is the primary objective of this study, is found in the hybrid circuit application of the unipolar insulated-gate field effect transistor and the bipolar high-efficiency switching transistor. The extremely high collector efficiency of the conventional switching-mode transistor r-f power generator when excited by a high input impedance MOSFET exciter, can enhance the overall stage efficiency with negligibly small exciting power. By choosing a high f_T, high β, low R_s switching transistor and

a high transconductance insulated-gate field-effect transistor combination, an r-f power generator with very high dc-to-ac conversion efficiency can be designed.

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13. ABSTRACT

Field effect transistors have several characteristics which are distinct from those of standard bipolar transistors. In this paper a study is made to see if any of these characteristics can be advantageously utilized to generate r-f power. (U)

A conventional class-C FET r-f power amplifier is analyzed following a semigraphical method similar to that used for vacuum tubes. Some advantageous characteristics of the device are discussed along with some drawbacks. (U)

The applicability of FETs to pulse-excited r-f power generation circuits is investigated and the device limitations in this field of application are discussed. (U)

Finally, the combined use of an FET and a conventional bipolar transistor, to overcome the respective limitations, in an efficient r-f power generation circuit is studied. A practical working model of this hybrid circuit was built to illustrate its advantages. (U)

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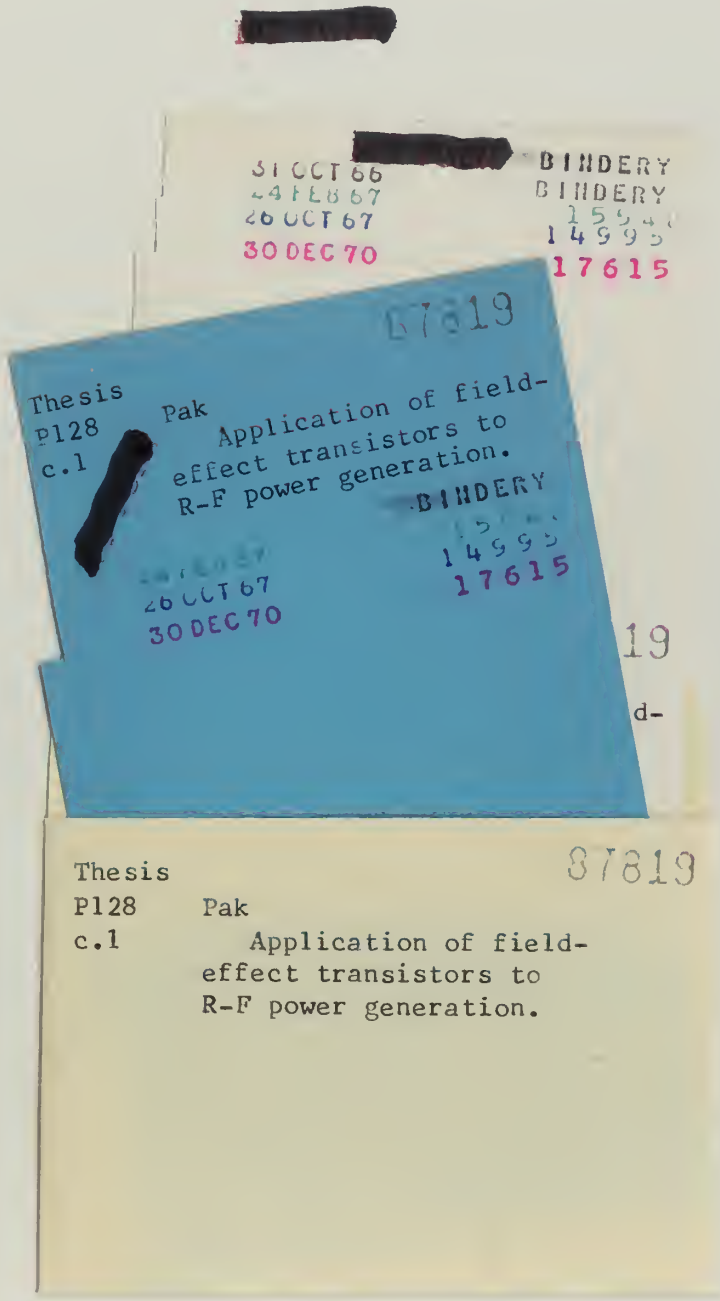
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